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Figure 1 (a)-(e) shows cross sectional views after various sequential steps in a copper damascene/CMP process: a patterned low dielectric constant material disposed on a silicon wafer to form a plurality of trenches is shown in Figure 1(a); a diffusion barrier layer covering the wafer surface, including the trenches is shown in Figure 1(b); a copper or copper alloy layer deposited thereon is shown in Figure 1(c) and the structure shown in FIG. 1(c) having the overburden portion removed by first CMP step to expose the barrier layer in the overburden regions is shown in Figure 1(d); a second CMP step then polishes the barrier layer and produces the completed structure shown in Figure 1(e).

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